# NCP5810

# Dual 1 W Output AMOLED Driver Supply

The NCP5810 is a dual−output DC/DC converter which can generate both a positive and a negative voltage. Both PWM converters achieve high efficiency for portable application. Thanks to the high output voltage accuracy and signal integrity the NCP5810 is particularly suitable for powering applications such as AMOLED display drivers. The output voltage of the inverter is fully configurable using external feedback resistors, where the output voltage of the boost is internally fixed. The switching regulator operates at 1.75 MHz which allows the use of small inductors and ceramic capacitors. In addition both converters are internally compensated which simplifies the design and reduces the PCB component count. Cycle−by−cycle peak current limit and thermal shut down provide value added features to protect the device. The NCP5810 is housed in low profile space−efficient 3x3 mm LLGA packages.

### Features

- High Overall Efficiency: 83% (Refer to Figure 4)
- Low Noise 1.75 MHz PWM DC/DC Converter
- Positive Output Fixed + 4.6 V
- Negative Output from − 2.0 to − 15.0 V
- High Output Voltage Accuracy
- Excellent Line Transient Rejection
- Soft Start to Limit Inrush Current
- Enable Control Facility with True−Cutoff
- Small LLGA 3x3 mm Packages
- These are Pb−Free Devices

### Typical Applications

- AMOLED Driver Supply
  - Cellular Phones
  - MP3 Player
  - Digital Cameras
  - Personal Digital Assistant and Portable Media Player
  - GPS

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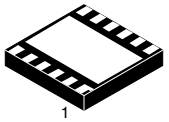
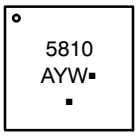
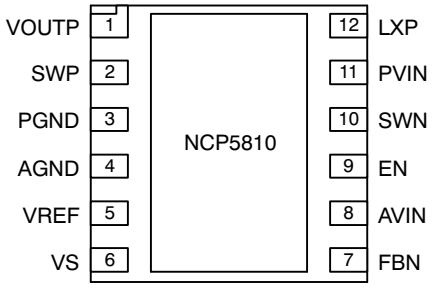



**12 PIN LLGA**
**MU SUFFIX**
**CASE 513AD**

**MARKING DIAGRAM**




5810 = Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)




(Top View)
12−pin 3 x 3 x 0.55 mm LLGA

Exposed pad must be soldered to PCB Ground plane

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

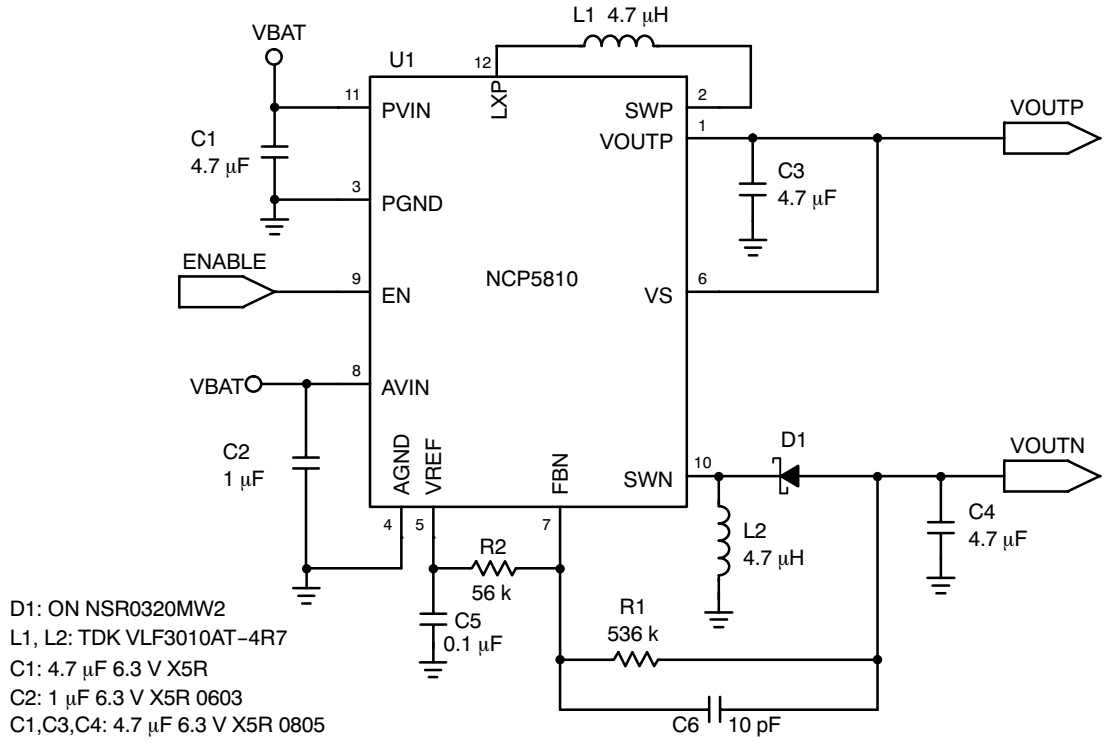



**Figure 1. Typical Application Circuit**

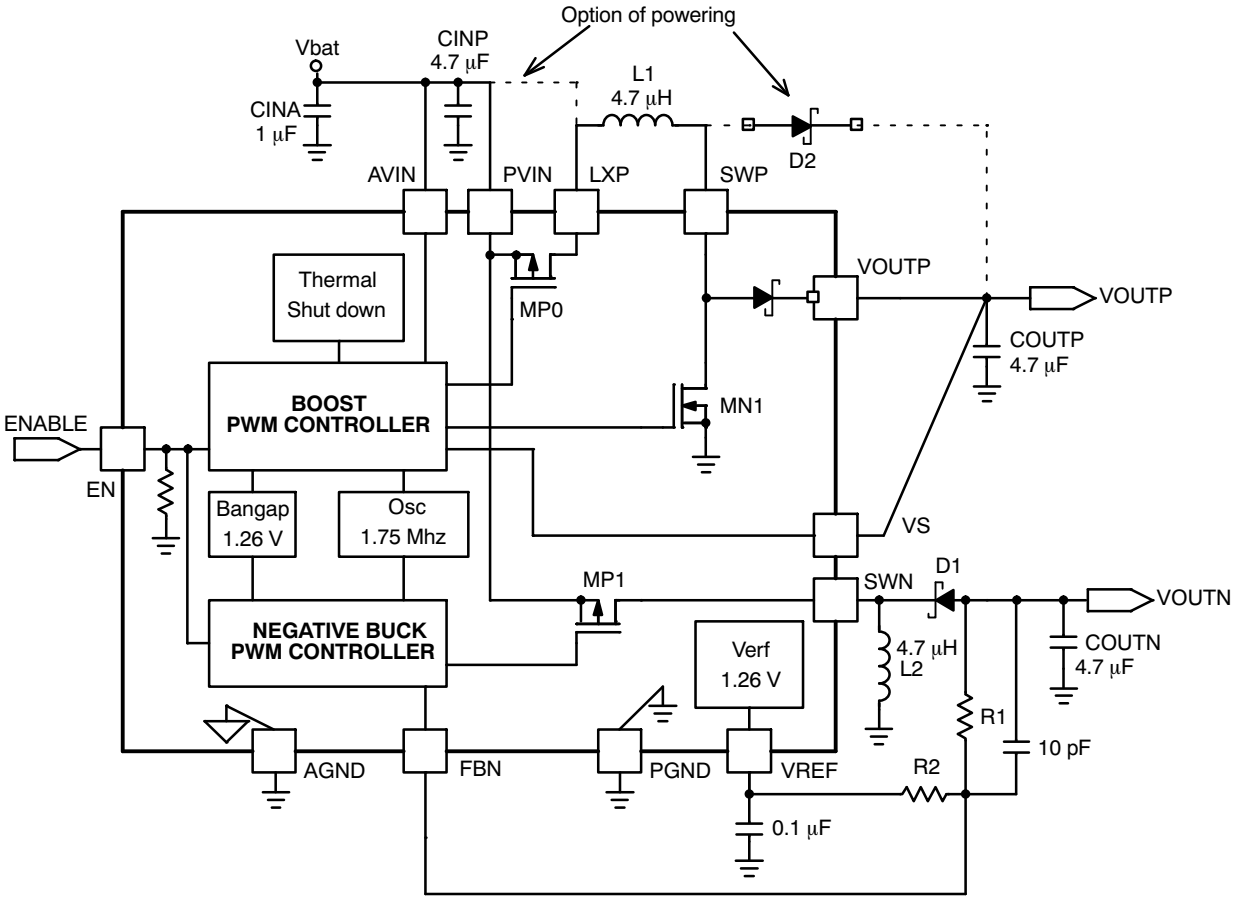



**Figure 2. Simplified Block Diagram**

**PIN FUNCTION DESCRIPTION**

| Pin | Pin Name | Type | Description |
|---|---|---|---|
| 1 | VOUTP | OUTPUT | **Positive Power Output:** A filter capacitor is necessary on this pin for the stability of the loop, to smooth the current flowing into the load, and limit the noise created by the fast transients present in this circuitry. A 4.7 μF ceramic bypass capacitor to GND is recommended. Care must be observed to avoid EMI through the PCB copper tracks connected to this pin. |
| 2 | SWP | POWER | **Switch LXP:** Positive power switch pin where one end of the L1 inductor is connected. Typical application uses a 4.7 μH inductor. |
| 3 | PGND | POWER | **Power Ground:** This pin is the power ground and carries the high switching current. A high quality ground must be provided to avoid any noise spikes/uncontrolled operation. Care must be observed to avoid high−density current flow in a limited PCB copper track. |
| 4 | AGND | POWER | **Analog Ground:** This pin is the analog ground of the device notably used by VREF. |
| 5 | VREF | OUTPUT | **Voltage Reference:** This output provides a 1.265 V voltage reference used notably for the negative feedback resistive network. |
| 6 | VS | INPUT | **Positive Output Voltage Sense:** This pin is the output voltage sense input for the positive boost converter and must be connected to COUTP bypass capacitor. |
| 7 | FBN | INPUT | **Feedback Negative:** This pin is the feedback voltage input for the negative Buck−Boost inverter. The middle point of a resistive bridge divider must be connected here. The resistive network must be connected between VREF and the anode of external Schottky. |
| 8 | AVIN | POWER | **Analog Power Supply:** The external voltage supply is connected to this pin. A 4.7 μF ceramic capacitor must be connected across this pin and the power ground to achieve the specified output power parameters. |
| 9 | EN | INPUT | **Enable:** An active high logic level on this pin enables the circuit. A built−in pull−down resistor disables the device if the pin is left open. Also in disable condition the device provides a true cut−off from PVIN to VOUTP and SWN. |
| 10 | SWN | INPUT | **Switch Negative:** Negative power switch pin where one end of the L2 inductor is connected. Typical application uses a 4.7 μH inductor. |
| 11 | PVIN | POWER | **Power Supply:** This pin is the power supply of the device. A 4.7 μF ceramic capacitor or larger must bypass this input to the ground. This capacitor should be placed as close as possible to this input. |
| 12 | LXP | POWER | **Switch LXP:** The inductor should be connected between this node and SWP. This output supplies power from PVIN and gives a true−cut off function in disable condition. |

**MAXIMUM RATINGS** (Note 1)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| AVIN and PVIN Pin: Power Supply Voltage (Note 2) | $V_{BAT}$ | 7.0 | V |
| EN Pin: Digital Logic Input (Note 2) | $V_{EN}$ | $-0.3 \le V_{IN} \le V_{BAT} +0.3$ | V |
| LXP Pin: Output (Note 2) | $V_{LXP}$ | $-0.3 \le V_{IN} \le V_{BAT} +0.3$ | V |
| VREF Pin: Output Reference Voltage (Note 2) | $V_{VREF}$ | $-0.3 \le V_{IN} \le V_{BAT} +0.3$ | V |
| VS Pin: Input (Note 2) | $V_{VS}$ | +17 | V |
| SWN Pin: Output (Note 2) | $V_{SWN}$ | −17 | V |
| SWP Pin: Input (Note 2) | $V_{SWP}$ | 9.8 | V |
| VOUTP Pin: Output (Note 2) | $V_{VOUTP}$ | +17 | V |
| FBN Pin: Input (Note 2) | $V_{FBN}$ | $-0.3 \le V_{IN} \le V_{BAT} +0.3$ | V |
| Human Body Model (HBM) ESD Rating are (Note 3) | ESD HBM | 2000 | V |
| Machine Model (MM) ESD Rating are (Note 3) | ESD MM | 200 | V |
| Digital Input Voltage<br>Digital Input Current | EN | $-0.3 \le V_{IN} \le V_{BAT} +0.3$<br>1 | V<br>mA |
| LLGA 3x3 mm package (Notes 6 and 7)<br>Thermal Resistance Junction−to−Case | $R_{\theta JC}$ | 12 | °C/W |
| Operating Ambient Temperature Range | $T_A$ | −40 to +85 | °C |
| Operating Junction Temperature Range | $T_J$ | −40 to +125 | °C |
| Maximum Junction Temperature | $T_{JMAX}$ | +150 | °C |
| Storage Temperature Range | $T_{STG}$ | −65 to +150 | °C |
| Moisture Sensitivity (Note 5) | MSL | Level 1 | |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTES:

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at $T_A$ = 25°C
2. According to JEDEC standard JESD22−A108B.
3. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115 for all pins.
4. Latchup Current Maximum Rating: ±100 mA per JEDEC standard: JESD78., class II
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.
6. The thermal shutdown set to 165°C (typical) avoids irreversible damage on the device due to power dissipation.
7. The $R_{\theta CA}$ is dependent on the PCB heat dissipation. The maximum power dissipation ($P_D$) is dependent on the min input voltage, the max output current and external components selected.

$$R_{\theta CA} = \frac{125 \ - \ T_A}{P_D} - R_{\theta JC}$$

**ELECTRICAL CHARACTERISTICS** Min & Max Limits apply for $T_A$ between −40°C to +85°C and $V_{IN}$ between 2.7 V to 4.6 V (Unless otherwise noted). Typical values are referenced to $T_A$ = +25°C and $V_{IN}$ = 3.7 V (Unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **POSITIVE BOOST DC/DC CONVERTER** | | | | | |
| Positive Operational Output Voltage Range | $V_{OUTP}$ | 4.55 | 4.6 | 4.65 | V |
| Maximum Inductor Peak Current | $I_{PEAKP\_MAX}$ | 530 | 700 | 800 | mA |
| Switches P0 ON Resistance | $P0_{MOS}$ $R_{DSON}$ | – | 320 | 640 | mΩ |
| Switches N1 ON Resistance | $N_{1MOS}$ $R_{DSON}$ | – | 300 | 600 | mΩ |
| Switches N1 Leakage Current<br>At $V_{IN}$ = 4.2 V | $N_{1MOS}$ L | – | 0.05 | 0.5 | μA |
| Efficiency (Notes 8, 9) | $E_{FF}$ | – | 85 | – | % |
| Positive Output Current Available (Notes 9, 10)<br>VIN ≥ 3.1 V<br>VIN ≥ 2.9 V, $T_A$ between 0 to +85°C | $I_{OUTP}$ | <br>0<br>0 | <br>270<br>– | <br>–<br>145 | mA |
| Output Voltage Line Regulation $I_{OUTP}$ = 0 mA<br>2.7 < $V_{IN}$ < 4.6 | $L_{INE\_RP}$ | – | – | 10 | mV |
| Output Voltage Line Transient Overshoot (Note 12) | $L_{INE\_TP}$ | – | 4 | – | mV |
| Power Supply Ripple Rejection (Notes 9, 13)<br>1.0 Hz to 1.0 kHz<br>1.0 kHz to 10 kHz | $P_{SRRP}$ | <br>–<br>– | <br>60<br>40 | <br>–<br>– | dB |
| Output Voltage Load Regulation (Note 14) | $L_{OAD\_RP}$ | – | – | 0.5 | %/100mA |
| Output Voltage Load Transient Response: Overshoot and Undershoot Vs. Steady State Voltage (Notes 9, 15) | $L_{TRP}$ | – | – | 100 | mV |
| **NEGATIVE BUCK DC/DC CONVERTER** | | | | | |
| Typical Negative Operational Output Voltage Range | $V_{OUTN}$ | −15 | – | −2.0 | V |
| Peak Inductor Current (Note 9) | $I_{PEAKN\_MAX}$ | 620 | 800 | 920 | mA |
| Switches P2 ON Resistance | $P_{2MOS}$ $R_{DSON}$ | – | 700 | 1400 | mΩ |
| Switches P2 Leakage Current<br>At $V_{IN}$ = 4.2 V | $P_{2MOS}$ L | – | 0.05 | 0.5 | μA |
| Efficiency (Notes 8, 9) | $E_{FF}$ | – | 80 | – | % |
| Negative Output Power Available (Notes 9, 10) @ $V_{OUTN}$ = −5.4 V<br>VIN ≥ 3.1 V<br>VIN ≥ 2.9, $T_A$ between 0 to +85°C | $P_{OUTN}$ | <br>–<br>0 | <br>175<br>– | <br>–<br>100 | mA |
| Output Voltage Reference 0 μA < $I_{REF}$ < 100 μA | $O_{VR}$ | −1 % | 1.265 | +1 % | V |
| Feedback Voltage Threshold in Steady State:<br>2.7 < $V_{IN}$ < 4.6 | $F_{BVN}$ | −2 % | 0.632 | +2 % | mV |
| Feedback Input Current | $F_{BICN}$ | −50 | – | 50 | nA |
| Output Voltage Line Regulation at $I_{OUTN}$ = 0 mA (Note 11)<br>2.7 < $V_{IN}$ < 4.6 | $L_{INE\_RN}$ | – | – | 20 | mV |
| Output Voltage Line Transient Overshoot (Note 12) | $L_{INE\_TN}$ | – | 4 | – | mV |
| Power Supply Ripple Rejection (Notes 9, 13)<br>1.0 Hz to 1.0 kHz<br>1.0 kHz to 10 kHz | $P_{SRRN}$ | <br>–<br>– | <br>60<br>40 | <br>–<br>– | dB |
| Load Regulation (Notes 11, 14) | $L_{OAD\ RN}$ | – | – | 0.5 | %/100mA |
| Load Transient Response: Overshoot and Undershoot Vs. Steady State Voltage (Notes 9, 15) | $L_{TRN}$ | – | – | 100 | mV |

**ELECTRICAL CHARACTERISTICS** (Min & Max Limits apply for $T_A$ between −40°C to +85°C and $V_{IN}$ between 2.7 V to 4.6 V. Typical values are referenced to $T_A$ = +25°C and $V_{IN}$ = 3.7 V, unless otherwise noted)

| Rating | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operational Power Supply | $V_{IN}$ | 2.7 | – | 4.6 | V |
| Internal Oscillator Frequency, $T_A$ = 25°C, $V_{IN}$ = 3.7 V | $F_{OSC}$ | 1.6 | 1.75 | 1.9 | MHz |
| Maximum Duty Cycle | $M_{DCY}$ | 87 | 90 | – | % |
| Stand by Current at $I_{OUTP}$ = $I_{OUTN}$ = 0 mA, EN = Low<br>$V_{IN}$ = 4.2 V, $T_A$ between 0 to +85°C | $I_{STB}$ | – | – | 2.0 | μA |
| Quiescent Current @ $V_{OUTN}$ = −5.4 V @ $T_A$ = +25°C<br>Switching (Note 9)<br>No Switching | $I_Q$ | <br>–<br>– | <br>1.5<br>1.0 | <br>3.0<br>– | mA |
| Soft Start Time to limit the Inrush Current | $S_{ST}$ | – | 1.0 | – | ms |
| Thermal Shut Down Protection | $T_{SD}$ | – | 165 | – | °C |
| Thermal Shut Down Protection Hysteresis | $T_{SDH}$ | – | 15 | – | °C |
| Voltage Input Logic Low | $V_{IL}$ | – | – | 0.4 | V |
| Voltage Input Logics High | $V_{IH}$ | 1.2 | – | – | V |
| EN pin Pull Down Resistance | $R_{ENP}$ | 280 | 400 | 670 | kΩ |

NOTES:

8. Efficiency is defined by 100 * (Pout / Pin), Vin = 3.1 to 4.2 V, L = VLF3010AT−4R7MR70 (DCR = 280 mΩ max, Isat = 700 mA), Load = 15 to 30 mA, Voutn = −5.4 V.
9. Guaranteed by design and characterized.
10. Typical application circuit and components depicted Figure 1.
11. Tested at 25°C and guaranteed from −40°C to +85°C by characterization.
12. Line drop and rise between 3.4 to 2.9 V in 50 μs at $I_{OUT}$ = 25 mA, $V_{OUTN}$ = −5.4 V.
13. Ripple = 0.2 V p−p at 25°C, Cout = 4.7 μF, $I_{OUT}$ = 0 to 100 mA, $V_{IN}$ = 3.7 V.
14. $I_{OUT}$ from 0 to 100 mA.
15. Load step 10 to 90 mA and 90 to 10 mA, rising and falling edge in 10 μs, Cout = 4.7 μF, $V_{IN}$ = 3.7 V.

## TYPICAL OPERATING CHARACTERISTICS

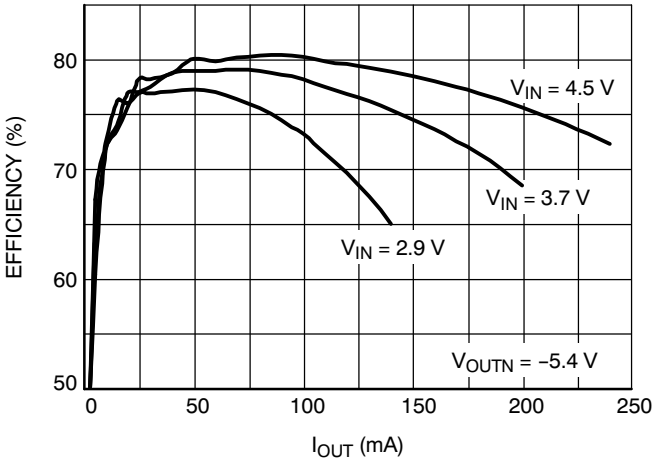



**Figure 3. Efficiency vs. $I_{OUT}$**
L = MARUWA CXFU0208−4R7

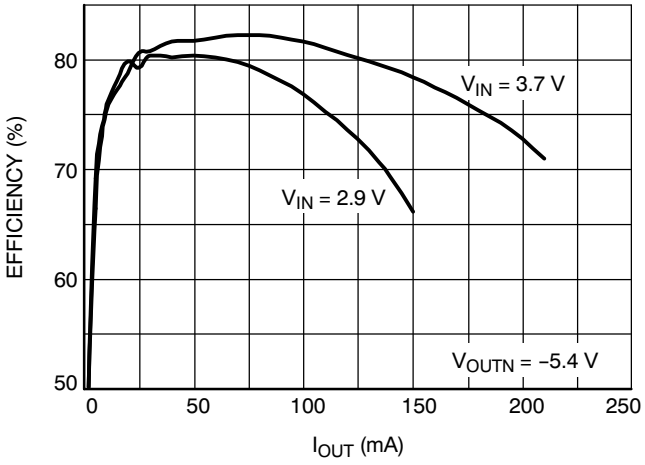



**Figure 4. Efficiency vs. $I_{OUT}$**, L = MARUWA
CXFU0208−4R7 plus Optional D2 NSR0320MW2

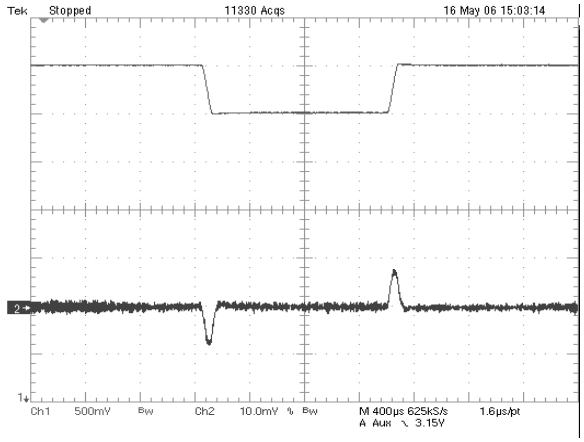



**Figure 5. Line Transient Response** $V_{OUTP}$ at 100 mA
1 VBAT, 500 mV/div DC, from 3.5 to 3.0 V in 50 μs
2 VOUTP, 10 mV/div AC, T = 400 μs/div

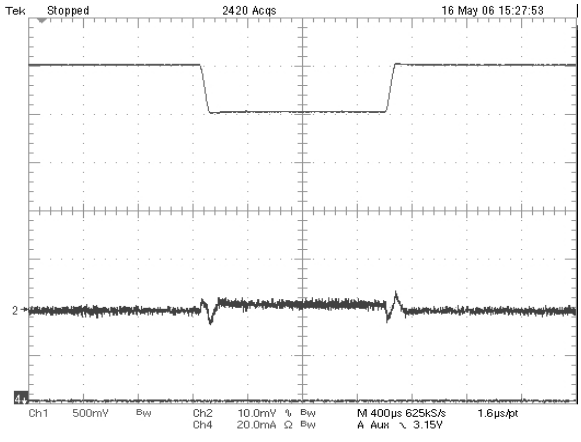



**Figure 6. Line Transient Response** $V_{OUTN}$ = −5.4 V,
100 mA 1 VBAT, 500 mV/div DC, from 3.5 to 3.0 V in 50 μs
2 VOUTN, 10 mV/div AC, T = 400 μs/div

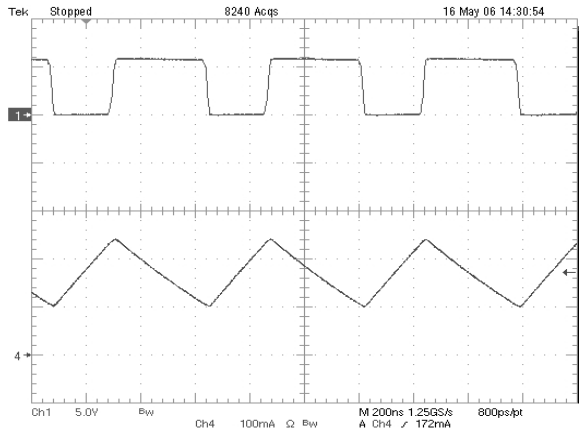



**Figure 7. Continuous Conduction Mode (CCM)**
1 SWP, 5 V/div DC, 4 $I_{LP}$, 100 mA/div, DC, $I_{OUTP}$ = 100 mA

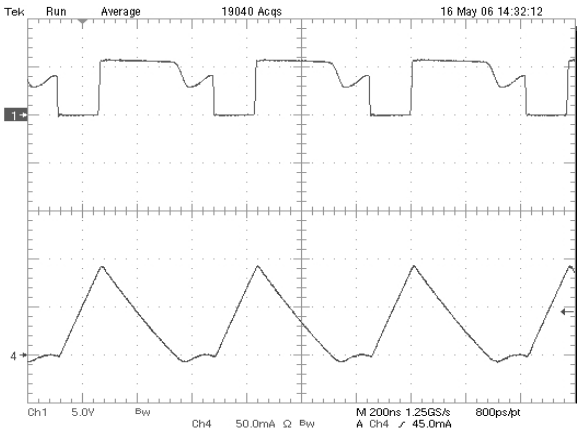



**Figure 8. Discontinuous Current Mode (DCM)**
1 SWP, 5 V/div, DC 4 $I_{LP}$, 50 mA/div, DC, $I_{OUTP}$ = 20 mA

Figures 7 and 8 have been done at VBAT = 3.7 V, $V_{OUTN}$ = −5.4 V

## TYPICAL OPERATING CHARACTERISTICS

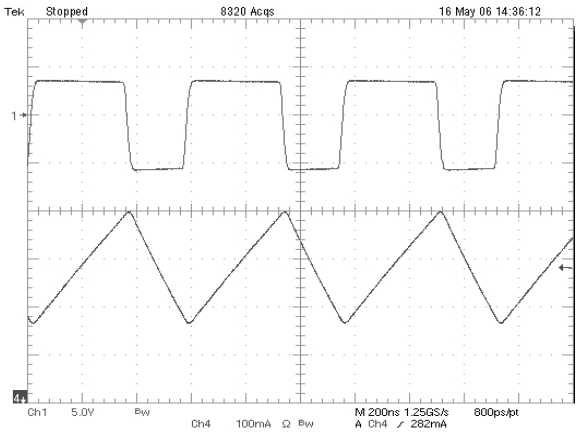



**Figure 9. Continuous Conduction Mode (CCM)**
1 SWN, 5 V/div DC, 4 $I_{LN}$, 100 mA/div, DC, $I_{OUTN}$ = 100 mA

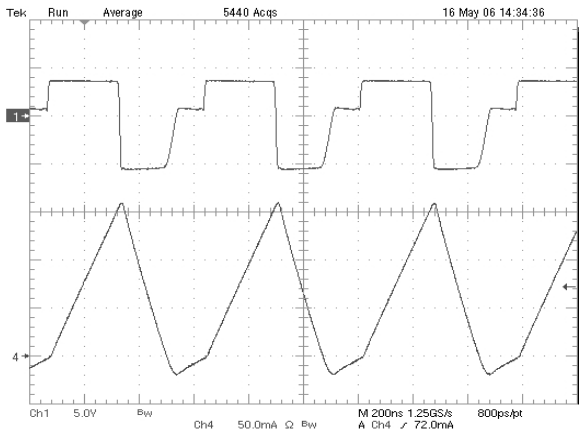



**Figure 10. Discontinuous Current Mode (DCM)**
1 SWN, 5 V/div, DC 4 $I_{LN}$, 50 mA/div, DC, $I_{OUTN}$ = 20 mA

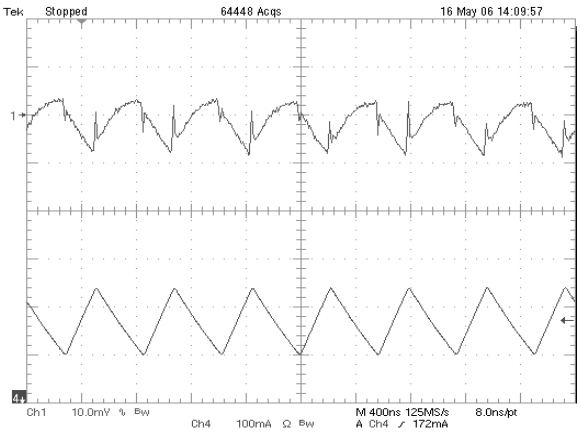



**Figure 11. Positive Output Voltage Ripple in CCM**
1 $V_{OUTP}$, 10 mV/div AC, 4 $I_{LP}$, 100 mA/div DC, $I_{OUTP}$ = 100 mA

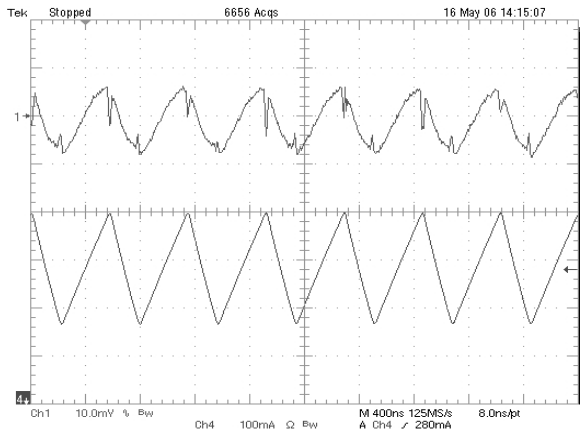



**Figure 12. Negative Output Voltage Ripple in CCM**
1 $V_{OUTN}$, 10 mV/div AC, 4 $I_{LN}$, 100 mA/div DC, $I_{OUTN}$ = 100 mA

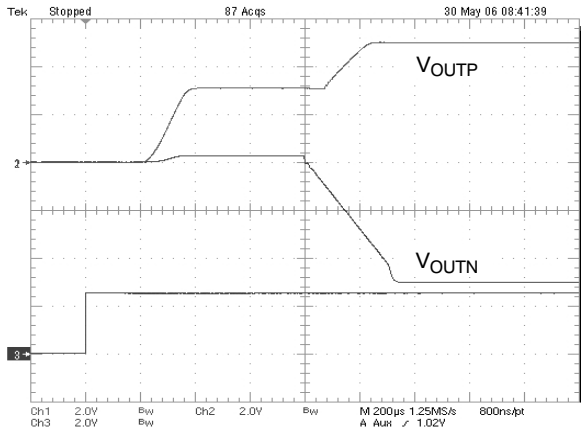



**Figure 13. Start−Up After Enable**
1 VOUTP, 2 V/div, 2 VOUTN, 2 V/div, 3 EN pin, 2 V/div

Figures 9 through 12 have been done at VBAT = 3.7 V and schematic depict Figure 1

## DETAILED OPERATING DESCRIPTION

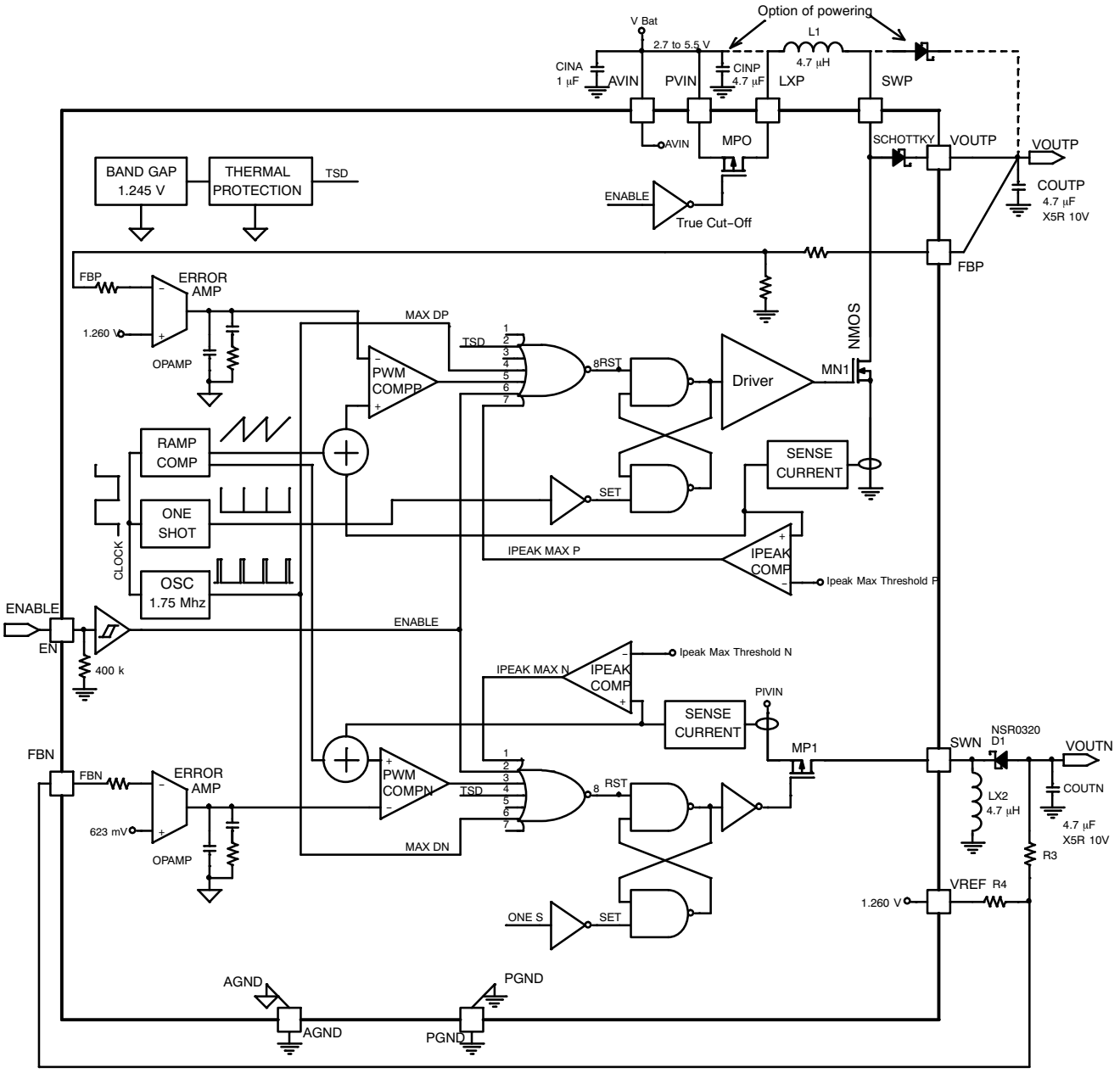



**Figure 14. Functional Block Diagram**

### Detailed Descriptions

The NCP5810 is a dual−output DC/DC converter which can generate both a positive and a negative voltage. The output voltage of the inverter is fully configurable using external feedback resistors. The switching regulator operates at 1.75 MHz which allows the use of small inductors and ceramic capacitors. The both converters are internally compensated which simplifies the design and reduces the PCB component count. Cycle−by−cycle peak current limit and thermal provide value added features to protect the device.

### Boost Operation

The internal oscillator provides a 1.75 MHz clock signal to trigger the PWM controller on each rising edge (SET signal) which starts a cycle. During this phase the low side MN1 switch is turned on thus increasing the current through the inductor L1. The switch current is measured by the SENSE CURRENT and added to the RAMP COMP signal. Then PWM COMPP compares the output of the adder and the signal from ERROR AMP. When the comparator threshold is exceeded, the MN1 power switch is turned off until the rising edge of the next clock cycle. In

addition, there are five functions which can reset the flip−flop logic to switch off the MN1. The MAX DP monitors the pulse width and if it exceeds 88% (nom) of the cycle time the switch will be turned off. This limits the switch from being on for more than one cycle. IPEAK COMP compares the sensed inductor current with the IPEAK_MAX threshold set at 700 mA (nom). If the current exceeds this value, the controller turns off the NMOS switch for the remainder of the cycle. This is a safety function to prevent any excessive current that could overload the inductor and the power stage. The boost regulator is internally compensated and provides a minimum of 45° phase margin.

### Buck−Boost Inverter Operation

Figure 9 depicts the two intervals of the buck−boost operation in Continuous Conduction Mode (CCM) in a simplified way. During the first interval, the internal PMOS power switch is turned on and the external Schottky diode is reverse biased. The inductor stores energy through the battery while the load is supplied by the output capacitor to maintain regulation. During the second interval, the switch is turned off and the diode is forward biased, this allows the energy stored in the inductor to be supplied to both the load and the capacitor.

In CCM, the voltage ratio of a buck−boost inverter converter can be expressed as:

$$\frac{V_{OUT\_N}}{V_{IN}} = \frac{D}{1 - D} \text{ where } D = \frac{T_{ON}}{T_{SW}}$$

The internal oscillator provides a 1.75 MHz clock signal to trigger the PWM controller on each rising edge (SET signal) which starts a cycle. During this phase the high side PMOS switch is turned on thus increasing the current through the inductor. The switch current is measured by the SENSE CURRENT and added to the RAMP COMP signal. Then PWM COMPN compares the output of the adder and the signal from ERROR AMP. When the comparator threshold is exceeded, the PMOS power switch is turned off until the rising edge of the next clock cycle. In addition, there are five functions which can reset the flip−flop logic to switch off the NMOS. The MAX DUTY CYCLE COMP monitors the pulse width and if it exceeds 88% (nom) of the cycle time the switch will be turned off. This limits the switch from being on for more than one cycle. IPEAK COMP compares the sensed inductor current with the IPEAK_MAX threshold set at 800 mA (nom). If the current exceeds this value, the controller turns off the PMOS switch for the remainder of the cycle. This is a safety function to prevent any excessive current that could overload the inductor and the power stage.

### Buck−Boost Compensation

Basically the buck−boost inverter is internally compensated and provides a minimum of 45° phase margin. But a 10 pF (C6) feed−forward capacitor is needed to improved stability with $C_{OUTN}$ = 4.7 μF (C4) used to bypass VOUTN. Moreover in order to achieve excellent the line transient rejection in critical conduction mode two 10 μF X5R in parallel for $C_{OUTN}$ can be used. In this case the feed−forward capacitor (C6) must be change from 10 pF to 68 pF as depicted Figure 15.

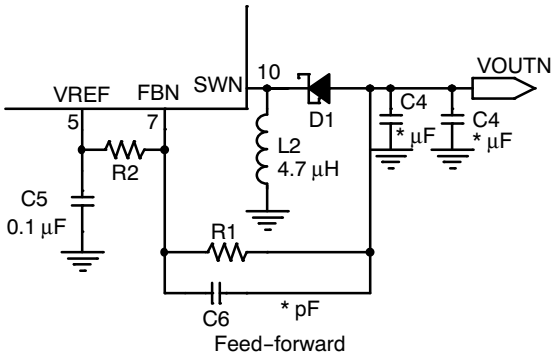



**Figure 15. Inverter Compensation**

### High Output Voltage Accuracy

NCP5810 integrates a very accurate internal voltage reference (1% nom). Combined with the use of precision feedback resistors, the NCP5810 will achieve highly precise output voltages.

### Excellent Line Transient Rejection and High Power Supply Rejection Ratio

High output voltage accuracy and signal integrity makes the NCP5810 the perfect solution for biasing Active Matrix OLED displays. In order to have a steady, clean display, OLEDs have to be biased by a very accurate voltage with high immunity to line and load transients. Both regulators have been specifically designed with high loop gain and high phase margin to satisfy the great constraints of AMOLED driving.

The boost converter features a high power supply rejection ratio of 60 dB (nom).

PSRR is defined by

$$-\ 20\text{LOG}\left(\frac{\text{OutputRipple}}{\text{VinRipple}}\right)$$

### Enable

This input logic allows enabling and disabling the converter. An active high logic level on this pin enables the device. A built−in pull−down resistor disables the device if the pin is left open.

### True Shut Down

When in disable condition, the switch MP0 is turned off and truly isolates the battery from the output. The True shut down eliminates the leakage current from the battery to the load and significantly reduces battery consumption during disable condition, thus increasing battery life.

### Inrush Current Limiting Circuitry

Before the NCP5810 boost converter is turned on, it is unknown whether the output capacitor COUTP is charged

or discharged. If the output capacitor is discharged, a common boost converter shows high inductor inrush current at start−up. The internal circuitry of the NCP5810 has been carefully designed to limit the amplitude of the inrush current at start−up.

### Thermal Shutdown

When the IC junction temperature exceeds 165°C (nom), the power section of the device is disabled. Normal operation will resume when the junction temperature drops below 150°C (nom).

## Design Procedure

### Buck−Boost Inverter Output Voltage Setting

The output voltage of the buck−boost inverter is also adjusted using external feedback resistors, and can be set from −2 V down to −15 V. Unlike for the boost converter, the lower feedback resistor R2 does not use the ground as a reference but uses the reference voltage (nom 1.265 V). R2 is placed between the feedback pin FBN (nom 632 mV) and the reference pin REF. As for the boost converter, the current flowing out of the feedback resistors must be as low as possible to ensure high efficiency in low load conditions. Nevertheless the feedback resistor impedance must not be too high to keep good voltage accuracy. Therefore it is recommended to use values in the 10 kΩ to 100 kΩ range for the lower resistor R2. The upper feedback resistor R1 can calculated using the following equation:

$$R_1 = R_2 \times \left( \frac{V_{OUTN} - V_{FBN}}{V_{FBN} - V_{REF}} \right)$$

$$\text{But : } V_{FBN} = \frac{V_{REF}}{2}$$

$$\text{So: } R_1 = R_2 \times \left( 1 + \frac{2 \times |V_{OUTN}|}{V_{REF}} \right)$$

For example, should one need –5.4 V for $V_{OUTN}$, if a 56 kΩ ±1% is selected of R2, R1 should be selected according to the following equation:

$$R_1 = 56 \times \left( 1 + \frac{2 \times 5.4}{1.265} \right) = 536\ k\Omega\ \pm 1\%$$

### Inductor Selection

Three different electrical parameters need to be considered when selecting an inductor, the absolute value of the inductor, the saturation current and the DCR. During normal operation, the NCP5810 is intended to operate in Continuous Conduction Mode (CCM). The two equations below can be used to calculate the peak current for each converters:

$$I_{PEAK\_P} = \frac{I_{OUT\_P}}{\eta_P \times (1 - D_P)} + \frac{V_{IN} \times D_P}{2 \times L_P \times F}$$

For the boost converter

$$I_{PEAK\_N} = \frac{I_{OUT\_N} \times D_N}{\eta_N \times (1 - D_N)} + \frac{V_{IN} \times D_N}{2 \times L_N \times F}$$

For the buck−boost inverter

Where $V_{IN}$ is the battery voltage, $I_{OUT\_X}$ is the load current, L the inductor value, F the switching frequency, and $D_X$ the duty cycle.

The global converter efficiency η varies with load current. A good approximation is to use η = 0.8 from the boost and η = 0.75 for the buck−boost inverter. It is important to ensure that the inductor current rating is high enough such that it not saturate. As the inductor size is reduced, the peak current for a given set of conditions increases along with higher current ripple so it is not possible to deliver maximum output power at lower inductor values. Finally an acceptable DCR must be selected regarding losses in the coil and must be lower than 300 mΩ to limit excessive voltage drop. In addition, as DCR is reduced, overall efficiency will improve. The inductor value should range between 2.7 μH and 6.8 μH, typically for each DC/DC converter, it is recommended to use a 4.7 μH low profile inductor. Some recommended inductors include but are not limited to:

TDK: VLF3010AT−4R7MR70 (1.0 mm)

TDK: MLP3216S2R7T (0.6 mm)

SUMIDA: CDH2D09BNP (1.0 mm)

MARUWA CXFU0208−4R7 (0.8 mm)

### Schottky Diode Selection

An external diode is required for the rectification of the negative output. The reverse voltage rating of the selected diode must be equal to or greater than the difference between the output voltage of the inverter and the input voltage. The average current rating of the diode must be greater than the maximum output load current. The peak current rating must be larger than the maximum peak inductor current. It is recommended to use a Schottky diode with lower forward voltage to minimize the power dissipation and therefore to maximize the efficiency of the converter.

Also a particular care must be observed for parasitic capacitance versus reverse voltage and leakage current versus junction diode temperature. Both parameters are impacting the efficiency in low load condition and switching quiescent current.

Some recommended Schottky diodes include but are not limited to:

ON SEMICONDUCTOR: NSR0320MW2

ON SEMICONDUCTOR: RB521S30

ROHM: RSX051VA−30

PHILIPS: PMEG2005AEL

### Input and Output Capacitors

$C_{OUTP}$ and $C_{OUTN}$ store energy during the $T_{OFF}$ phase and sustain the load during the $T_{ON}$ phase. In order to minimize the output ripple, typically a 4.7 μF low ESR multi−layer ceramic capacitor type X5R is recommended. Moreover two 10 μF in parallel can be used to improved the line transient rejection in critical conduction mode of the inverter in this case see recommendation in Buck−Boost Compensation paragraph. To achieve high performances (signal integrity) one 4.7 μF 6.3 V X5R should be used to bypass the power input supply $C_{INP}$ (PVIN) and one 1.0 μF 6.3 V X5R to bypass the analog input supply $C_{INA}$ (AVIN).

Also a particular care must be observed for DC−bias effects in ceramic capacitor. Actually smaller the case−size and higher the DC bias voltage, the bigger drop in capacitance. For a stability viewpoint the percentage drop in capacitance for the chosen input or output operating voltage must be limit to 20%.

Some recommended capacitors include but are not limited to:

4.7 μF 6.3 V 0603
TDK: C1608X5R0J475MT
TDK: CGB4B1X5R0J475M (0.5 mm)

4.7 μF 10 V 0805
TDK: C2012X5R1A475MT
MURATA: GRM219R61A475KE

10.0 μF 6.3 V 0805
TDK: C2012X5R0J106M (0.95 mm max)

10.0 μF 10 V 0805
TDK: C2012X5R1A106MT (1.25 mm)

### Layout Recommendations

The high speed operation of the NCP5810 demands careful attention to board layout and component placement. To prevent electromagnetic interference (EMI) problems and reduce voltage ripple of the device any high current copper trace which see high frequency switching should be optimized. Therefore, use short and wide traces for power current paths and for power ground tracks.

In this application both couples of elements formed by the Schottky diode D1 / capacitor C4 and D2 (optional) / C3 are in the high frequency switching path where current flow is discontinuous. These components (D1/C4) in one hand and (D2/C3) in other hand should be placed as close as possible to reduce parasitic inductance connection. Also it is important to minimize the area of the SWP and SWN nodes and used the ground plane under them to minimize cross−talk to sensitive signals and IC. The exposed pad of the package must be connected to ground plane of the board that is important for EMI and thermal management. Also, PGND and AGND pin connection must be connected to the ground plane. In addition, the inductors track connection L1, L2 and input bypass capacitor C1, C2 must be placed shortly to the NCP5810 pins connection to reduce EMI. Finally it is always good practice to keep the sensitive tracks such as feedback connection (VS and FBN) away from switching signal connections (SWP and SWN) by laying the tracks on the other side of PCB. Figure 16 show an example of optimized PCB layout.

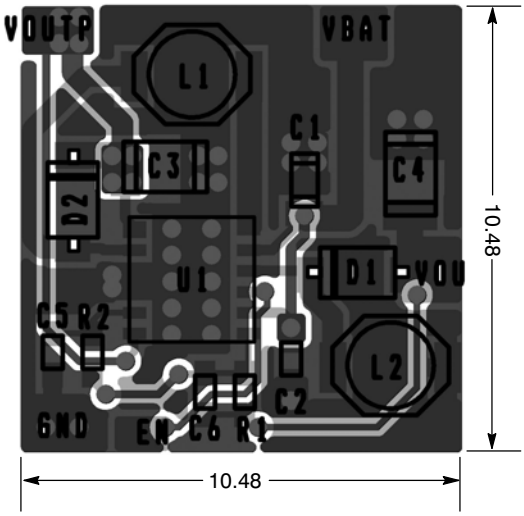



**Figure 16. Recommended PCB Layout**

### Thermal Considerations

Careful attention must be paid to the internal power dissipation of the NCP5810. The power dissipation is a function of efficiency and output power. Hence, increasing the output power requires better components selection. For example, should one change inductors: larger inductor value (in micro Henri) and/or lower DCR may improve efficiency. Adding the optional Schottky diode D2 provides a lower drop when the current flowing from the inductor to the load, thereby improving the boost converter efficiency.

The exposed thermal pad that is designed to be soldered to the ground plane to used the PCB as a heatsink. This ground should then be connected to an internal copper ground plane with thermal via placed directly under the package to spread out the heat dissipated by the NCP5810 as depicted in Figure 16**.**

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NCP5810MUTXG | LLGA−12 3x3 mm (Pb−Free) | 3000 / Tape & Reel |

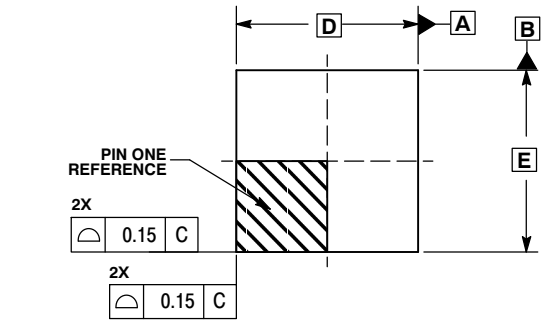
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Demo Board Available:

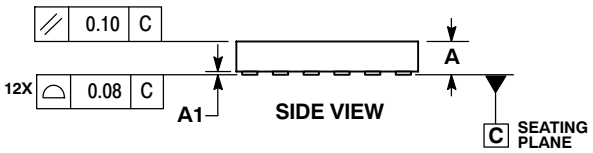
- The NCP5810GEVB/D evaluation board that configures the device in typical application to supply constant voltage.

## PACKAGE DIMENSIONS

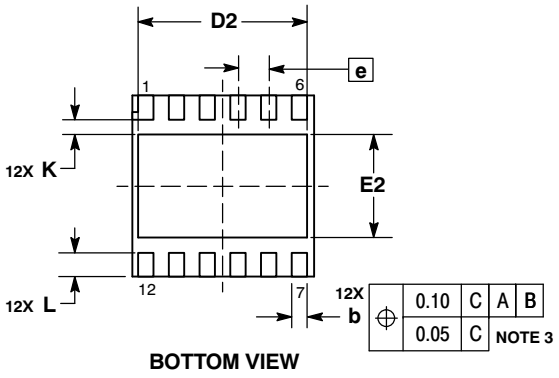
**12 PIN LLGA**
**MU SUFFIX**
CASE 513AD
ISSUE A




TOP VIEW




SIDE VIEW

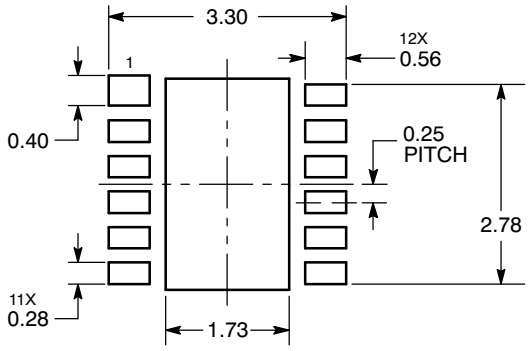



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.50 | 0.60 |
| A1 | 0.00 | 0.05 |
| b | 0.20 | 0.30 |
| D | 3.00 BSC | |
| D2 | 2.75 | 2.85 |
| E | 3.00 BSC | |
| E2 | 1.65 | 1.75 |
| e | 0.50 BSC | |
| K | 0.20 | --- |
| L | 0.35 | 0.45 |

### SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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